## REMARKS

Claims 1-33 were pending. By this response, please amend claims 1, 2, 3 16, 31, please cancel claims 6, 20, 32, 33.

### Objections

The Examiner objected to the drawings for not showing every feature of claims 32 and 33. Claims 32, 33 have been canceled.

The Examiner objected to claim 33. Claim 33 has been canceled.

### Claim Rejections

The Examiner rejected claim 2 under 35USC112, first paragraph, as allegedly failing to comply with the enablement requirement. The Examiner stated "the disclosure doe not disclose how this "replica signal" is generated to additionally supply this signal to each sample and hold circuit."

Claim 2 has been amended. The specification on page 2 describes replica signals. Figure 5 shows a sample and hold circuit receiving the previously describe replica signal, and shows sampled and hold versions of the replica signal being subtracted from corresponding versions of the sample and hold receive signals. One skilled in the art can practice amended claim 2 based on the descriptions of the specification.

The Examiner rejected claim 20 under 35USC112, second paragraph, as allegedly being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Claim 20 has been canceled.

Claims 1-6, 8-11, 16-17, 20, 24-27 were rejected under 35 U.S.C. §102(b) as allegedly being anticipated by U.S. Patent No. 4,811,342 to Huang.

Amended claim 1 includes the following features:

1 to N sample and hold circuits, each sample and hold circuit receiving a first signal comprising a far-end signal and an echo signal., wherein each of the N sample and hold circuits receives one of N clock signals, and wherein a phase of each of the N clock signals relative to the other (N-1) clock signals is dependent on the value of N; and

a plurality of subtraction circuits, each subtraction circuit receiving an output of at least one of the sample and hold circuits, each subtraction circuit subtracting at least a fraction of a sampled and hold replica signal from at least a fraction of the output of the at least one of the sample and hold circuits.

In contrast, Huang teaches an echo canceller that stores echo signals in a plurality of sample and hold circuits. The echo signals are selectively switched to the input of a summing amplifier for subtraction from a data plus echo signal. A training sequence detector is utilized to detect the statistical occurrence of a predetermined training signal embedded within a stream of data.

Applicants respectfully disagree with the Examiner's rejection for the following reasons;

1. Huang does not include subtracting a sampled and hold replica signal from a sample and hold receive (first) signal.

Rather, Huang subtracts and echo signal from a data plus echo signal. Huang shows in Figure 2, a sample and hold circuit 88 receiving a transmit and receive signals, and a shift register 52 receiving a transmit signal. A training sequence is detected by a training

sequence detector. A sampled and hold replica signal is not subtracted from a sampled and hold receive signal.

2. None of the cited references teach a sample and hold replica signal.

Applicant's claimed include a sample and hold replica signal. Huang does not teach a replica signal, much less, a sample and hold replica signal.

3. Huang does not control clocking the sample and hold signals (of the first signal and the replica signal) with N clock signals, and wherein a phase of each of the N clock signals relative to the other (N-1) clock signals is dependent on the value of N.

The sample and hold circuits 88, 92, 94, 96, 98 of Huang are not controlled by clocked signals having a controlled a predictably controlled phase. The phase of the clocks of Huang are in not way dependent upon the number of sample and hold circuits N.

Claim 16 includes the feature sampling and holding N versions of a replica signal-with the N clock signals. None of the cited references teach sample and hold versions of the replica signal with a N clock signals in which a phase of each of the N clock signals relative to the other (N-1) clock signals is dependent on the value of N.

Amended claims 1 and 16 are patentable over the cited references.

Claim 31 includes similar features, and therefore, is patentable over the cited references as well.

Claims 2-15, 17-19, 21-30 comprise additional patentable features. Claims 2-15, 17-19, 21-30 are directly or indirectly dependent on claims 1, 16. Therefore, claims 2-15, 17-19, 21-30 are patentable over the cited references.

**Conclusion**

The Applicant respectfully requests that all pending claims be allowed.

By responding in the foregoing remarks only to particular positions taken by the Examiner, the Applicant does not acquiesce with other positions that have not been explicitly addressed. In addition, Applicant's arguments for the patentability of a claim should not be understood as implying that no other reasons for the patentability of that claim exist.

For all of the reasons set forth above, it is urged that the application is in condition for allowance, an indication of which is respectfully solicited.

If there are any outstanding issues that might be resolved by an interview or an Examiner's amendment, the Examiner is requested to call Applicant's representative at the telephone number shown below.

Respectfully submitted,

Date: July 23, 2007

Brian Short

Brian Short
Reg. No. 41,309

Teranetics, Inc.
PO Box 641867
San Jose, CA 95164-1867

Teranetics-1001